AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A method of determining the load of the gates driven by a logic gate divided by the size of the logic gate, *i.e.*, the fanout, for at least one transistor fanout, the method comprising:

    a) creating a sizing model by replacing at least one logic element in a circuit description with a sizing element that includes a resistor that dynamically varies based upon one or more values in the sizing model, *i.e.*, a dynamic resistor;

    b) determining a steady state solution to the sizing model;

    c) determining the size of at least one transistor; and

    d) determining at least one transistor the fanout for at least one transistor from the steady state solution.

2. (Original) The method of claim 1, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor the size of which is based at least upon a current.

3. (Original) The method of claim 1, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor the size of which is based at least upon the logical effort of a logical element.

4. (Original) The method of claim 1, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor the size of which is based at least upon a voltage.

5. (Original) The method of claim 1, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor the size of which is based at least upon a current and a voltage.

6. (Original) The method of claim 1, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor the size of which is based at least upon the logical effort of a logic element, a current, and a voltage.

7. (Original) The method of claim 1, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor the size of which is proportional to the square root of a current.

8. (Original) The method of claim 1, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor the size of which is proportional to the square root of the logical effort of a logic element.

9. (Original) The method of claim 1, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor

the size of which is proportional to the square root of the inverse of a voltage.

10. (Currently Amended) A device containing machine-readable instructions, that when executed perform a method of determining at least one ratio of the size of a first transistor with respect to the size of a second transistor transistor sizes, the method comprising:

    a) creating a sizing model by replacing at least one logic element in a circuit description with a sizing element that includes a resistor that dynamically varies based upon one or more values in the sizing model, *i.e.*, a dynamic resistor;

    b) determining a steady state solution to the sizing model; and

    c) determining the ratio of the size of the first transistor with respect to the size of the second transistor at least one transistor fanout from the steady state solution.

11. (Original) The device of claim 10, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor the size of which is based at least upon a current.

12. (Original) The device of claim 10, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor the size of which is based at least upon the logical effort of a logical element.

13. (Original) The device of claim 10, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor

the size of which is based at least upon a voltage.

14. (Original) The device of claim 10, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor the size of which is based at least upon a current and a voltage.

15. (Original) The device of claim 10, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor the size of which is based at least upon the logical effort of a logic element, a current, and a voltage.

16. (Original) The device of claim 10, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor the size of which is proportional to the square root of a current.

17. (Original) The device of claim 10, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor the size of which is proportional to the square root of the logical effort of a logic element.

18. (Original) The device of claim 10, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor the size of which is proportional to the square root of the inverse of a voltage.

19. (Currently Amended) An integrated circuit created at least in part by a method of determining at least one ratio of the size of a first transistor with respect to the size of a second transistor ~~transistor sizes~~, the method comprising:

   a) creating a sizing model by replacing at least one logic element in a circuit description with a sizing element that includes a resistor that dynamically varies based upon one or more values in the sizing model, i.e., a dynamic resistor;

   b) determining a steady state solution to the sizing model; and

   c) determining the ratio of the size of the first transistor with respect to the size of the second transistor ~~at least one transistor fanout~~ from the steady state solution.

20. (Original) The integrated circuit of claim 19, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor the size of which is based at least upon a current.

21. (Original) The integrated circuit of claim 19, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor the size of which is based at least upon the logical effort of a logical element.

22. (Original) The integrated circuit of claim 19, wherein creating a sizing model includes replacing at least one logic element in the circuit description with a sizing element that includes a dynamic resistor the size of which is based at least upon a voltage.